CLAIMS

1. A cellular inverter generating an alternating electrical voltage from a succession of various serial combinations of DC voltage electrical sources (V1, V2, ..., VN) and comprising a series of several elementary cells (C1, C2, ..., CN) and a switching control unit (10), the elementary cells (C1, C2, ..., CN) having a bridge structure with a controlled switch (STi, SBi, STib, SBib) in each of the branches of the bridge and a DC voltage electrical source (Vi) in a first diagonal of the bridge, and being interconnected within the series via the second diagonal of their bridge structure, the switching control unit (10) delivering the control commands for the controlled switches (STi, SBi, STib, SBib) of the various elementary cells (Ci) and comprising a high-frequency switch-mode voltage regulation circuit (100) and a circuit (200) for selecting the serial combination of the DC voltage electrical sources (Vi) of the elementary cells (Ci) in service, the switch-mode voltage regulation circuit (100) operating so as to minimize an error signal that is representative of the difference existing between the electrical voltage (Vout) present across the ends of the series of cells (Ci) and a variable voltage setpoint (Vref) sampling a model form of alternating voltage, and generating signals indicating arrival at upper and lower limits of its range of operation (I, D), the combination selection circuit (200) being controlled by means of the signals indicating arrival at upper and lower limits of range of operation (I, D) delivered by the high-frequency switch-mode voltage regulation circuit (100), said cellular inverter being characterized in that its switching control unit (10) comprises a high-frequency switch-mode voltage regulation circuit equipped with a pre-compensation device (107, 108) that is controlled by the signals indicating arrival at upper and lower limits of range

of operation (I, D) and that corrects its lag during a voltage jump caused by a change of the serial combination of DC voltage electrical sources currently in use.

2. The inverter as claimed in claim 1, characterized in that the pre-compensation circuit (10) takes into account the values of the voltage jumps associated with the combination changes undertaken by the combination selection circuit (200), the combination change moments indicated by the limit reach signals (I, D) and the reaction time of the high-frequency switch-mode voltage regulation circuit (100).

3. The inverter as claimed in claim 1, characterized in that the pre-compensation device (107, 108) comprises a compensation form generator (107) controlled by means of the limit reach signals (I, D) from the switch-mode voltage regulation circuit (100) and an adder circuit (108) that adds the compensation form delivered by the compensation form generator circuit (107) to a signal (Sc) from the high-frequency switch-mode voltage regulation circuit (100) fixing the duration of a chopping period assigned to the conduction.

4. The inverter as claimed in claim 1, characterized in that the pre-compensation device (107, 108) comprises a compensation form generator (107) controlled by means of the limit reach signals (I, D) from the switch-mode voltage regulation circuit (100) and of a signal (ad) coming from the combination selector (200) that provides data on the amplitude of the voltage jump accompanying each change of serial combination, and an adder circuit (108) adding the compensation form delivered by the compensation form generator circuit (107) to a signal (Sc) from the high-frequency switch-mode voltage regulation circuit (100)

fixing the duration of a chopping period assigned to the conduction.

5. The inverter as claimed in either of claims 3 or 4, characterized in that the compensation form generator circuit (108) is a memory storing, in sampled form, various forms of compensation established by experimentation for each combination change generated by the combination selection circuit (200).

6. The inverter as claimed in claim 3, characterized in that the compensation form generator circuit (107) is a memory that contains compensation forms associated with the DC voltage jumps encountered during the combination changes and that is addressed by an addressing circuit deducing, from the limit reach signals (I, D), the DC voltage jump corresponding to the combination change carried out by the combination selection circuit (200).